

# Quantum Mechanical Modeling of the Charge Distribution in a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si P-Channel MOSFET

Michael J. Hargrove<sup>†</sup>, Albert K. Henning<sup>†</sup>, James A. Slinkman<sup>‡</sup>, and John C. Bean<sup>§</sup>

<sup>†</sup>Thayer School of Engineering, Dartmouth College, Hanover, New Hampshire 03755

<sup>‡</sup>IBM Microelectronics Division, Essex Junction, Vermont 05452

<sup>§</sup>AT&T Bell Laboratories, Murray Hill, NJ 07974

## ABSTRACT

Incorporation of a Si<sub>1-x</sub>Ge<sub>x</sub> alloy layer in the channel of a p-channel MOSFET has been proposed as a means to improve device performance [1, 2]. In order to achieve optimal performance in such a device, the inversion charge distribution must be located in the alloy channel layer where the carrier mobility is highest [3]-[6]. The smaller bandgap of the Si<sub>1-x</sub>Ge<sub>x</sub> alloy layer, compared to Si, creates a potential well in which the carriers can reside. Understanding how the carriers distribute themselves under various gate bias conditions is necessary in order to achieve optimal device design. Our purpose here is to demonstrate the dependence of the charge distribution in a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel MOSFET based on the self-consistent solution of the Schrödinger-Poisson equations.

## INTRODUCTION

Quantum mechanical modeling of the charge distribution in a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel MOSFET (SiGe PFET) is presented. The results are based on a fully self-consistent solution of the one-dimensional, time-independent, Schrödinger and Poisson equations. The purpose of this work is to demonstrate the dependence of the charge distribution in a SiGe PFET on the Si surface channel thickness ( $T_{Si}$ ), the Si<sub>1-x</sub>Ge<sub>x</sub> channel width ( $T_{SiGe}$ ), and the Ge mole fraction in the Si<sub>1-x</sub>Ge<sub>x</sub> alloy channel ( $x$ ).

The performance improvement of a SiGe PFET structure is dependent upon how the charge distributes itself under various gate bias conditions. Since Si<sub>1-x</sub>Ge<sub>x</sub> layers have been shown to have increased carrier mobility compared to conventional Si-only layers [2], optimizing the charge distribution in the Si<sub>1-x</sub>Ge<sub>x</sub> channel region of the SiGe PFET is critical. Previous studies [7] have relied on classical solution techniques which do not adequately describe the quantum mechanical nature of the carrier confinement. This work accounts for the quantum mechanical effects of carrier confinement in the Si surface channel and the Si<sub>1-x</sub>Ge<sub>x</sub> buried channel region by calculating the quantized energy subbands, wave functions, charge density, and electrostatic potential, self-consistently. We describe the effects of variations in the physical construction of the device, and calculate the quantized energy level

separation as a function of surface carrier concentration,  $N_s$ .

## DEVICE STRUCTURE

The Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel FET device under study is shown in Fig. 1. The critical device design parameters are

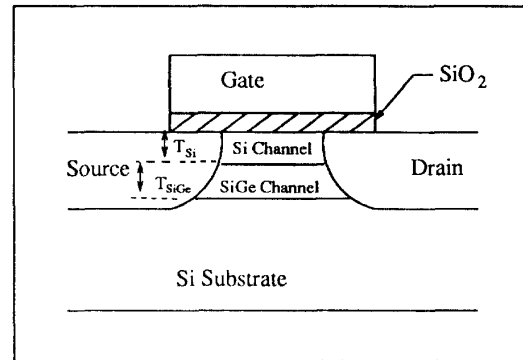


Figure 1: Cross-section of a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel MOSFET, showing the Si surface channel and Si<sub>1-x</sub>Ge<sub>x</sub> channel thickness.

$T_{Si}$ ,  $T_{SiGe}$ , and the Ge mole fraction ( $x$ ) in the Si<sub>1-x</sub>Ge<sub>x</sub> alloy. The device can be fabricated with conventional processing, including MBE formation of the Si<sub>1-x</sub>Ge<sub>x</sub> layer. The energy band diagram for such a device, biased near inversion, is shown in Fig. 2. The valence band offset,  $\Delta E_v$ , is related to the Ge mole fraction ( $x$ ) by the empirical relation  $\Delta E_v \approx 0.74x$  [6]. From a quantum mechanical viewpoint, in order to maximize the charge distribution in the Si<sub>1-x</sub>Ge<sub>x</sub> quantum well where mobility is highest, the resulting valence band offset must be larger than the resulting Si inversion channel depth formed at the Si/SiO<sub>2</sub> interface, and given by  $V_o$ . As will be shown, minimizing  $T_{Si}$  is also necessary to ensure optimal carrier confinement in the alloy channel. By locating the inversion charge in the alloy channel the resulting current drive of the device should be maximized, which, for a given drain bias, should also maximize device transconductance.

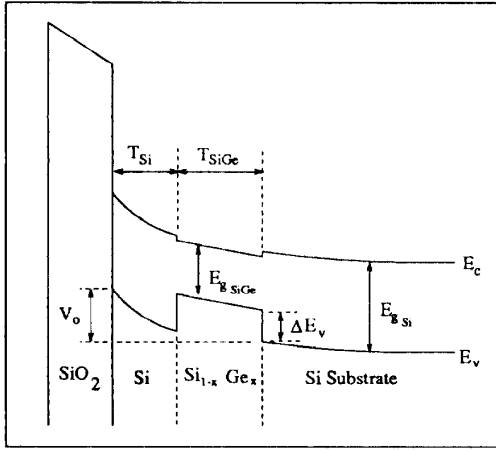


Figure 2:  $Si/Si_{1-x}Ge_x/Si$  energy band biased near inversion, with substrate doping of  $N_d = 7 \times 10^{16} \text{ cm}^{-3}$ .

### NUMERICAL APPROACH

In order to account for the quantum mechanical effects of carrier confinement in the Si surface well and the  $Si_{1-x}Ge_x$  buried channel layer, a fully self-consistent solution of the Schrödinger-Poisson equations must be considered. The 1D, time-independent Schrödinger equation, is given by

$$\frac{d}{dz} \left( \frac{1}{m^*(z)} \frac{d\psi_n(z)}{dz} \right) + \frac{2}{\hbar^2} [E_n - V(z)] \psi_n(z) = 0 \quad (1)$$

$\psi_n(z)$  is the wave function solution,  $E_n$  is the eigen-energy,  $V(z)$  is the spatially distributed potential,  $\hbar$  is Planck's constant divided by  $2\pi$ , and  $m^*(z)$  is the carrier effective mass. The solution is determined by a two-directional numerical Runge-Kutta (RK) algorithm [8] which provides a fourth-order accurate solution for arbitrary well configurations. The results of the Schrödinger solution provide the quantized eigen-energies and corresponding wave functions which determine the charge density. The hole charge density,  $p(z)$ , is given by

$$p(z) = \sum_n N_n |\psi_n(z)|^2 \quad (2)$$

where  $N_n$  is the number of holes per subband, and is given by

$$N_n = \int_{E_n}^{\infty} g_{2D}(E) f(E) dE \quad (3)$$

where  $g_{2D}(E)$  is the 2D density of states function and  $f(E)$  is the Fermi-Dirac distribution function. The resulting expression for  $N_n$  is

$$N_n = \frac{k_B T m^*}{\pi \hbar^2} \ln \left[ 1 + \exp \left( \frac{E_F - E_n}{k_B T} \right) \right] \quad (4)$$

The resulting charge density,  $p(z)$ , is then coupled to Poisson's equation, given by

$$\frac{d^2 V(z)}{dz^2} = \frac{4\pi e^2}{\epsilon} (p(z) + N_a^- - N_d^+) \quad (5)$$

where  $N_a^-$  and  $N_d^+$  are the ionized impurity distribution, and  $\epsilon$  is the material dielectric constant (here we assume the electron charge density is zero). The Poisson equation is solved by a standard finite difference method in order to provide the self-consistent potential,  $V(z)$ .

The boundary conditions for the two-directional RK method are specified within the  $Si_{1-x}Ge_x$  quantum well, and provide for wave function continuity at the prescribed patchpoint, as well as continuity of its first derivative. These boundary conditions result in a determinant formulation whose sign change indicates a bracketed eigen-energy solution. A combination of a binary search followed by a Regula-Falsi search results in the eigen-energy determination. The two-directional RK method is advantageous since it provides the ability to simulate arbitrary quantum well configurations with spatially varying physical parameters, and eliminates the computation and evaluation of derivatives which are required in any Taylor series based methods, such as the Numerov technique [9]. It also provides the ability to include continuum states which can not be calculated with typical matrix eigenvalue solution techniques.

### NUMERICAL RESULTS

The figure of merit we use to establish the optimal design point of the SiGe PFET is the ratio of Si surface channel charge,  $Q_{Si}$ , to the charge in the  $Si_{1-x}Ge_x$  channel,  $Q_{SiGe}$ . The lower this ratio, the more total inversion charge resides in the  $Si_{1-x}Ge_x$  channel where carrier mobility is highest, resulting in optimal current drive and maximized transconductance. Fig. 3 shows the ratio of charge distribution as a function of gate bias, for different Si surface channel thicknesses. These results indicate that the Si surface layer should be on the order of 25 Å or less, in order to optimize the charge distribution in the SiGe channel region. The thickness of  $T_{Si}$  is post gate oxidation, which implies a deposited Si surface cap thickness large enough to accommodate gate oxide growth and the resulting Si consumption. Fig. 4 shows the charge ratio versus gate bias, as a function of Ge mole fraction in the SiGe channel. The simulations indicate that higher Ge mole fraction in the channel alloy, resulting in larger valence band offset, provides more carriers confined in the  $Si_{1-x}Ge_x$  channel. Large Ge-mole fraction in  $Si_{1-x}Ge_x$  alloys has been shown to cause alloy relaxation and misfit dislocation generation [10]. A careful balance between this process limit and an optimized device design must be struck in order to maximize the charge distribution within the SiGe quantum well. Our simulations indicate that a Si channel thickness of less than 25 Å (post gate oxidation), coupled with as large a Ge-mole fraction in the SiGe

## 30.3.2

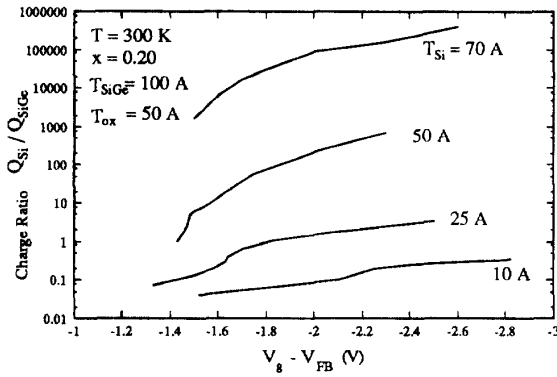


Figure 3: Plot of  $Q_{Si}/Q_{SiGe}$  versus gate bias, as a function of the Si surface channel thickness.

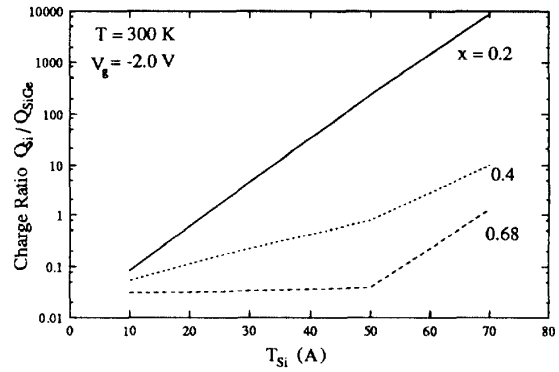


Figure 5: Plot of  $Q_{Si}/Q_{SiGe}$  versus  $T_{Si}$ , as a function of the Ge mole fraction ( $x$ ) in the  $Si_{1-x}Ge_x$  alloy channel, at  $V_g = -2.0$  V

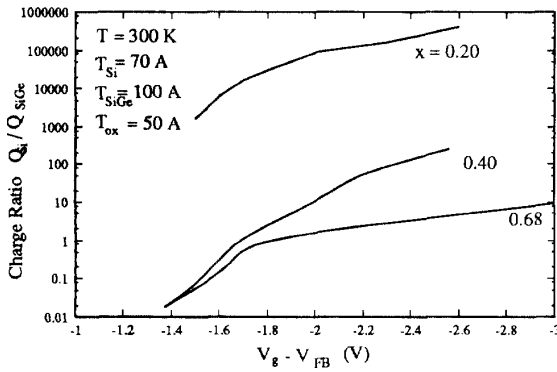


Figure 4: Plot of  $Q_{Si}/Q_{SiGe}$  versus gate bias, as a function of the Ge mole fraction ( $x$ ) in the  $Si_{1-x}Ge_x$  alloy channel.

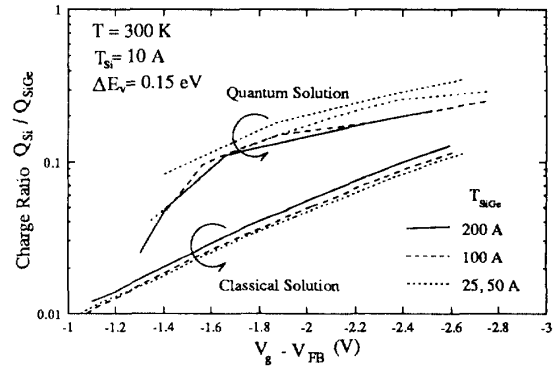


Figure 6: Plot of  $Q_{Si}/Q_{SiGe}$  versus gate bias, as a function of the  $Si_{1-x}Ge_x$  channel thickness,  $T_{SiGe}$ . Both the quantum-based solution and classical solution are shown.

alloy as possible, without generating misfit dislocations, provide the first steps toward an optimized SiGe PFET. Fig. 5 provides a design curve that indicates the charge ratio at specific  $T_{Si}$  and  $x$  values.

The  $Si_{1-x}Ge_x$  alloy thickness is a function of the Ge mole fraction [10]. The larger the value of  $x$ , the thinner  $T_{SiGe}$  must be in order not to exceed the critical layer thickness for misfit dislocation generation [10]. In MOSFET devices with tenth micron source/drain junction depths, the  $Si_{1-x}Ge_x$  channel thickness can be 100 Å or more, depending on the value of  $x$ , and the value of  $T_{Si}$ . Fig. 6 shows the dependence of the charge ratio on  $T_{SiGe}$ . At low gate bias the charge ratio is independent of  $T_{SiGe}$ , while at larger gate bias the smaller  $T_{SiGe}$  well shows an increased  $Q_{Si}/Q_{SiGe}$ . This effect is due to the combination of higher subband energies being populated at larger  $V_g$ , and the larger subband energy spacing of  $Si_{1-x}Ge_x$  channel wells with smaller  $T_{SiGe}$ , resulting in more charge

tunneling into the Si surface channel. Included in Fig. 6 is a classical Poisson solution. The classical results are achieved using a numerical solution to Poisson's equation, applied to the Si/ $Si_{1-x}Ge_x$  system [11]. The technique is based on the method of [12], modified to allow discontinuities in conduction and valence bands according to the electron affinity rule [13]. The classical solution results in an underestimate of the charge ratio, and illustrates the need for a complete quantum-mechanical based solution in order to fully understand the carrier confinement effects. Charge ratios for the quantum-based solution are larger than those for the classical solution. Classically, charge is located close to the valence band edge, and cannot tunnel through the barrier between the surface Si well and the  $Si_{1-x}Ge_x$  well. The quantum solution requires greater band-bending in order to fill the subband energy levels, located relatively far from the valence band edge. It also

allows tunneling of charge from the  $\text{Si}_{1-x}\text{Ge}_x$  well into the Si surface layer. Both effects increase the  $Q_{\text{Si}}/Q_{\text{SiGe}}$  ratio.

The energy subband-splitting in the channel of a Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel MOSFET is shown in Fig. 7. The energy spacing is shown for a fixed  $T_{\text{Si}} = 10$  Å, and different values of  $x$  and  $T_{\text{SiGe}}$ . As  $N_s$  increases with larger gate bias, higher subband energies will become occupied. Fig. 7 shows a significant increase in the subband

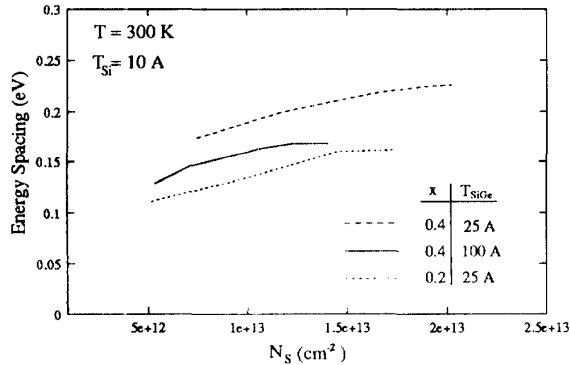


Figure 7: Subband energy spacing versus surface charge density, as a function of  $x$  and  $T_{\text{SiGe}}$ .

energy as  $x$  is increased from 0.2 to 0.4. The increase in  $x$  results in a deeper Si<sub>1-x</sub>Ge<sub>x</sub> channel well which increases the subband energy by approximately 50 meV. Decreasing the width of the Si<sub>1-x</sub>Ge<sub>x</sub> channel well also tends to increase the subband energy by approximately 25 meV.

### DISCUSSION

The results of the self-consistent solution of the Schrödinger-Poisson equations, applied to SiGe p-channel MOSFETs, establish a set of optimized physical design parameters which serve as a starting point in designing SiGe PFETs. The quantum mechanical nature of the carrier confinement effects in the Si surface channel and Si<sub>1-x</sub>Ge<sub>x</sub> channel wells, impose constraints on  $T_{\text{Si}}$ ,  $T_{\text{SiGe}}$ , and  $x$ . For optimal charge distribution within the SiGe PFET it has been shown that  $T_{\text{Si}}$  must be  $\leq 25$  Å, and the Ge mole fraction be  $\geq 40\%$ , resulting in  $T_{\text{SiGe}} \approx 100$  Å. The limitation on  $T_{\text{SiGe}}$  is based on the requirement of having  $x \geq 0.4$  in order to achieve a Si<sub>1-x</sub>Ge<sub>x</sub> well depth large enough to confine the holes, and therefore not exceed the critical layer thickness of the alloy and introduce misfit dislocations. An alternative approach to achieving larger valence band offset, while not sacrificing critical layer thickness, will be to grade the Ge mole fraction from some minimum value at the Si<sub>1-x</sub>Ge<sub>x</sub>/Si-substrate interface up to a maximum value ( $x \geq 0.4$ ) at the Si-surface/Si<sub>1-x</sub>Ge<sub>x</sub> interface [14, 15]. This technique allows for a large  $\Delta E_v$  where the carriers are confined, while enabling commensurate alloy growth.

### CONCLUSIONS

In summary, a fully self-consistent solution of the Schrödinger-Poisson equations, applied to Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si p-channel MOSFETs, has been described. The solution technique employs a two-directional Runge-Kutta algorithm with boundary conditions applied at a patchpoint within the quantum well, and a standard finite-difference solution of the coupled Poisson equation. The ratio of the charge distribution in the Si surface channel to the Si<sub>1-x</sub>Ge<sub>x</sub> channel is used as the figure of merit. Optimal device design is achieved by incorporating a very thin ( $\leq 25$  Å) Si surface layer coupled with a large ( $x \geq 0.4$ ) Ge mole fraction in the alloy. Very thin  $T_{\text{SiGe}}$  alloy layers ( $\leq 50$  Å) display larger charge ratios due to more carrier tunneling into the Si surface channel. The differences between the fully self-consistent solution and the classical Poisson solution are demonstrated by the quantitative underestimate of the charge ratio by the Poisson-only solution. The effect of strain,  $T_{\text{SiGe}}$ , and surface charge density on the subband energy spacing is also presented.

### ACKNOWLEDGMENTS

The authors would like to thank Dr. Emmanuel F. Crabbé for his valuable discussion, and Dr. Chuck E. Hembree for his help in establishing the Schrödinger-Poisson solver.

### REFERENCES

- [1] D. K. Nayak, *et al.*, *IEEE Electron Device Lett.* **12**, 4, 154, April 1991.
- [2] P. M. Garone, *et al.*, *IEDM Tech. Dig.*, p. 29, 1991.
- [3] P. M. Garone, *et al.*, *IEEE Electron Device Lett.* **12**, 5, 230, May 1991.
- [4] S. Subbanna, *et al.*, *Proc. Symp. VLSI Tech.*, p. 103, 1991.
- [5] S. Verdonckt-Vandebroek, *et al.*, *Proc. Symp. VLSI Tech.*, 1991, pp. 105-106.
- [6] R. People, *IEEE J. Quantum Electron.* **QE-22**, 1696 (1986).
- [7] P. M. Garone, *et al.*, *IEEE Electron Dev. Lett.* **13**, 56 (1992).
- [8] W. H. Press, *et al.*, *Numerical Recipes in C*, Cambridge University Press, 1988.
- [9] D. R. Hartree, *Numerical Analysis, 2nd Ed.*, Oxford University Press, 1958.
- [10] R. People and J. C. Bean, *Appl. Phys. Lett.* **48**, 538 (1986).
- [11] A. K. Henning, *Electro. Chem. Soc., Extended Abstracts* **1,404**, May 1991.
- [12] R. Jaeger, *et al.*, *ISSCC Dig. Tech. Papers*, p. 14, 1982.
- [13] R. L. Anderson, *Sol. St. Electron.* **5**, 341, 1962.
- [14] S. Verdonckt-Vandebroek, *et al.*, *IEEE Trans. Electron Devices* **41**, 1, 90, January 1994.
- [15] S. Voinescu and C. A. T. Salama, *Canadian J. Phys.* **70**, 975, 1992.