LATERAL DISTRIBUTION OF INTERFACE STATES IN PMOSFET'S

Judith L. Dimauro* and Albert K. Henning

Thayer School of Engineering, Dartmouth College
Hanover, New Hampshire 03755

*present address: Harris Corporation
1680 University Ave., Rochester, NY 14610

ABSTRACT

Precise measurements of the lateral distribution of interface states in PMOSFET's, before and after drain-avalanche-hot-carrier (DAHC) stress, are reported. The results are analyzed in the context of simultaneous gate current and substrate current measurements, and 2-D numerical simulations. Comparison of the results to similar NMOSFET measurements demonstrates electron injection across the Si-SiO_2 interface during DAHC stress creates amphoteric interface states along the drain-region interface; and negative trapped oxide charge along the channel-region interface.

INTRODUCTION

Accurate knowledge of lateral interface state densities is crucial to prediction of long-term MOSFET performance and reliability. Extensive measurements in NMOSFET's [1-5] have established the knowledge base used in several 2-D simulation tools to model the measured effects of lateral interface states in NMOSFET's [5,6], but none to date has incorporated effects in PMOSFET's, primarily due to limited experimental data [7].

We extract $N_{it}(x)$ from standard [2,8] charge-pumping measurements, using a novel calculation [9] on PMOSFET's which improves previous methods [4,7,10]. Specifically, $N_{it}(x)$ and not $\Delta N_{it}(x)$ is extracted, by making no assumption of N_{it} uniformity across the lateral, unstressed interface. Overly-simplified assumptions of the effect of interface states on capacitance [7], and the validity of substituting $D_{it}(x)$ for $N_{it}(x)$ in the calculation [10], are also avoided.

EXPERIMENTAL DETAILS

A conventional P-well CMOS technology was used to fabricate the devices used in this study. Oxide thickness is 385Å, the gate electrode is n^+ polysilicon, and the PMOS source-drain junctions are created from single-diffused B^{11} implants. Further details are given in [13]. I-V measurements were made using an HP 4142B. Frequency pulses used in the charge-pumping measurements were delivered by a Tektronix AFG 5101 pulse generator.

Charge-pumping current I_{CP}, drain current I_D, substrate current I_{SUB}, and gate current I_G were monitored before and after stress. DAHC stress was performed at V_D=-10V and V_G=-2.6V for the PMOS devices discussed here. NMOS stress conditions were V_D=6V and V_G=2V. Stress times were 120min. Tests were performed to determine if results from stress applied all at once differed from stress applied incrementally; no differences were noted.

RESULTS AND DISCUSSION

Figures 1 and 2 show the basic I_{CP} measurements leading to $N_{it}(x)$ extraction, an example of which is shown in Figure 3. PISCES [11] was used to correlate V_{SUB} and lateral position x [12]. The sign of I_{CP} is *opposite* that for NMOSFET's, indicating interface states are donor-like in PMOSFET's, and thus amphoteric overall. $N_{it}(x)$ is determined using a new calculation [9] which makes no assumptions about the existing lateral N_{it} distribution. The extracted $N_{it}(x)$ thus becomes an absolute, and not relative, value. Peak $N_{it}(x)$ is aligned with peak lateral electric field (at the stress voltage condition) at the channel surface. However, this is more fortunate coincidence than strict correlation. For the drain-avalanche hot carrier (DAHC) stress applied, minority carriers are generated downstream of the peak lateral field [13], but flow back toward the interface along the electric field lines [14], ending roughly above the point of maximum lateral field.

Figure 4 shows the effects of DAHC stress on PMOSFET I_{SUB}. In NMOSFET's for this type of stress, I_{SUB} is enhanced by a higher lateral electric field in the drain region. Such field enhancement is caused by negative charge near the Si-SiO_2 interface: the negative charge screens the positive gate bias, pushing the channel more deeply into saturation. Both negative N_{it} (due to negatively charged acceptors) and negative N_{ot} give rise to this charge. For the PMOSFET's here, I_{SUB} is suppressed, again consistent with negative charge, which in PMOSFET's decreases the lateral electric field by enhancing the inverting gate bias. This charge is due to N_{ot} since, as seen in Figures 1-3, the positive N_{it} are predominantly above the drain, and thus do not affect DC I_{SUB} measurements.

CH2865-4/90/0000-0081 $1.00 © 1990 IEEE

Figure 5 shows the effects of DAHC stress on $I_{G,e}$, and $I_{G,h}$. In NMOSFET's, $I_{G,e}$ is suppressed by this stress: the negative interfacial charge from both ionized acceptor N_{it}, and N_{ot} creates an increased barrier to electron injection. For PMOSFET's, $I_{G,e}$ is suppressed, and $I_{G,h}$ is enhanced, also consistent with negative N_{ot}, increase of the electron injection barrier, and decrease of the hole injection barrier. The positive, donor N_{it} are insufficient to affect the DC I_G measurements. In particular, note the change from net $I_{G,e}$ to $I_{G,h}$ for V_G<-4.1V. This is the channel hot hole (CHH) portion of the PMOSFET gate current characteristic, which cannot usually be seen because of the large ΔE_C in an unstressed device. However, with negative N_{ot} above both the DAHE and CHH injection points, the electron barrier is increased, and the hole barrier decreased, sufficient to show net $I_{G,h}$.

PISCES simulations confirm these conclusions. Figure 6 shows the simulation mesh, and metallurgical junction derived from a SUPREM [15] process simulation. Figures 7 and 8 show, respectively, the measured and simulated subthreshold I-V curves. The measured curve evidences increased N_{it} (increased subthreshold slope [16]) *and* increased electron N_{ot} (I_{DS} increase, and junction leakage increase in the lowest V_G regime). The simulation included only positive charge along the interface, using values from the extracted $N_{it}(x)$. As expected, little change is seen between stressed and unstressed simulations.

Experience in NMOSFET's [5] suggests the constant inversion V_G used during I_{CP} measurements causes an over-estimate of $N_{it}(x)$ in unstressed devices, since the back-biased-enhanced surface (vertical) electric field can increase state filling via the Poole-Frenkel effect [17]. At 300K, the surface field need only be enhanced by ten percent to cause a two-fold increase in I_{CP}. Figure 9 shows simulations of the vertical field near (but just outside) the PMOSFET drain. These simulations contradict the postulate of the Poole-Frenkel effect enhancing I_{CP} [5], since the vertical field increases only marginally during the trap filling portion of the I_{CP} cycle. Ten percent changes in vertical field are not experienced until a depth of more than 200Å into the channel is reached.

CONCLUSIONS

In summary, we have demonstrated the following. 1) Lateral interface state distributions in unstressed and stressed PMOSFET's have been measured with greater precision than previously. 2) Under DAHC stress, electron transport across the interface creates N_{it} above the drain, and N_{ot} above the channel, simultaneously. 3) From the sign of I_{CP}, the generated N_{it} are donor-like (positive above E_F, neutral below). Compared to observed acceptor-like I_{CP} in NMOSFET's, this reaffirms the amphoteric nature of interface states. 4) Substrate and gate current measurements demonstrate the presence of *negative* N_{ot}, in addition to N_{it}. 5) Comparison studies, both measurement and simulation, of NMOSFET's and PMOSFET's under DAHC stress show minority carriers generated by impact ionization in the drain (holes in NMOS, electrons in PMOS) generate N_{it}, while N_{ot} consist solely of *electrons*, regardless of device polarity. 6) Simulations of vertical field near the drain during the trap-filling part of the I_{CP} cycle suggest heavy doping, and not Poole-Frenkel effects, as the cause of increased N_{it} near the drain of unstressed devices.

ACKNOWLEDGEMENTS

The authors acknowledge gratefully support received through a Career Development Professorship from Analog Devices (Norwood, MA).

REFERENCES

[1] W.V. Backensto and C.R. Viswanathan, IEE Proc. **128** p. 44 (1981)
[2] G. Groeseneken, *et al.*, IEEE Trans. Elec. Dev. **ED-31**, p. 42 (1984)
[3] E. Takeda, *et al.*, IEEE Trans. Elec. Dev. **ED-30**, p. 675 (1983)
[4] H. Maes and G. Groeseneken, Elec. Lett. **18**, p. 372 (1982)
[5] M.G. Ancona, *et al.*, IEEE Trans. Elec. Dev. **ED-35**, p. 2221 (1988)
[6] F. Hofmann and W. Hänsch, J. Appl. Phys. **66**, p. 3092 (1989)
[7] R. Mahnkopf, *et al.*, J. Phys. Colloq. **49**, p. C4-775 (1988)
[8] P. Heremans, *et al.*, IEEE Trans. Elec. Dev. **ED-35**, p. 2194 (1988)
[9] J.L. Dimauro, M.S. Thesis, Dartmouth College (1989)
[10] C. Plossu, *et al.*, Sol. St. Comm. **65**, p. 1231 (1988)
[11] M. Pinto, *et al.*, Stanford (U.) Elec. Lab Tech. Rep. (1984)
[12] T. Poorter and P. Zoestbergen, IEEE-IEDM Tech. Dig., p. 100 (1984)
[13] A.K. Henning, Ph.D. Dissertation, Stanford University (1987)
[14] A.K. Henning, ECS Proc. Vol. **89-7**, p. 385 (1989)
[15] S.E. Hansen, "SUPREM-III User's Manual-Version 8628", Stanford University (1986)
[16] E.H. Nicollian and J.R. Brews, *MOS Physics and Technology*, New York: J. Wiley (1982)
[17] E. Rosencher, *et al.*, J. Appl. Phys. **57**, p. 2823 (1985)

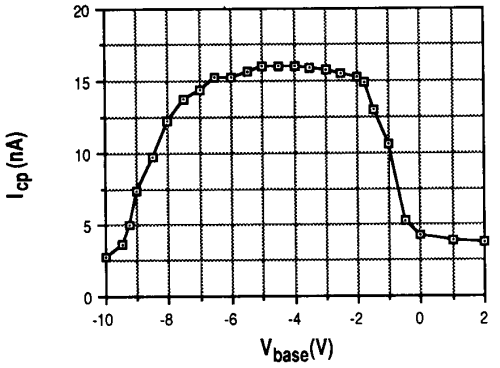

Figure 1: Characteristic 'flat-bell' charge-pumping curve obtained from standard techniques [2]. Measurement done here on a PMOSFET with W = 25μm, L_{eff} = 3.7μm. Device fabrication described in [13].

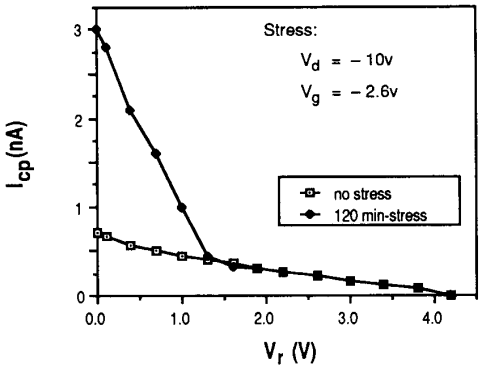

Figure 2: Characteristic charge-pumping current versus reverse substrate bias, before and after DAHC stress. PMOSFET with W = 25μm, L_{eff} = 1.7μm.

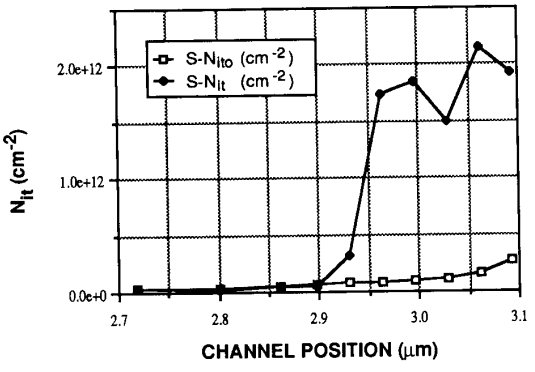

Figure 3a: Extracted N_{it} before and after DAHC stress for the same device as in Figure 2. PMOSFET metallurgical junction shown in Figure 3b.

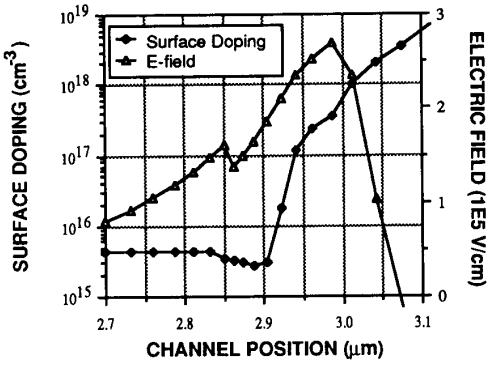

Figure 3b: Lateral electric field and doping concentration versus channel position along the Si-SiO_2 interface. The peak electric field occurs well inside the drain metallurgical junction, located at a channel position of 2.89μm. Field is shown for the same device seen in Figures 2 and 3a, for the DAHC stress condition V_D = −10V, V_G = −2.6V.

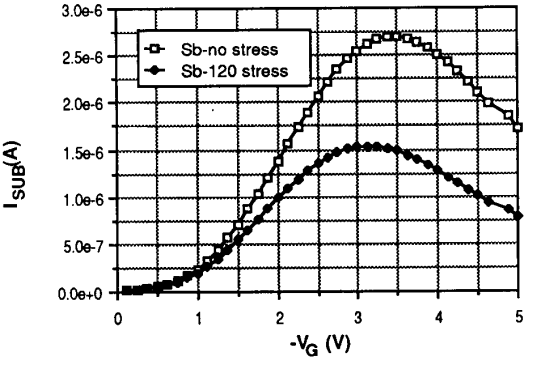

Figure 4: Measured substrate current vs. gate voltage for the device of Figures 2-3, with V_D = −10V. Suppression of the substrate current after stress results from weakening of the lateral electric field, consistent with electron trapping above the device channel.

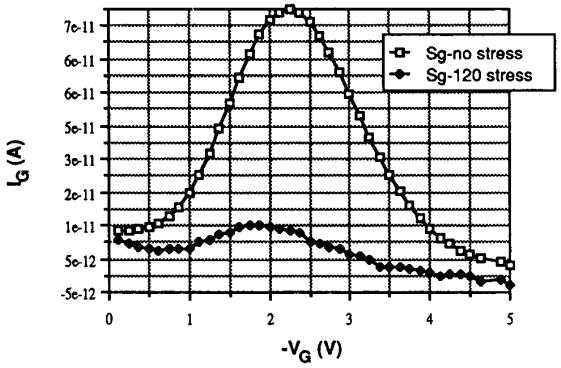

Figure 5: Measured gate current characteristic for the device of Figures 2-4, for $V_D = -10V$. Positive I_G corresponds to electron gate current; note the change to hole current after the DAHC stress at higher V_G, enabled by trapped electrons.

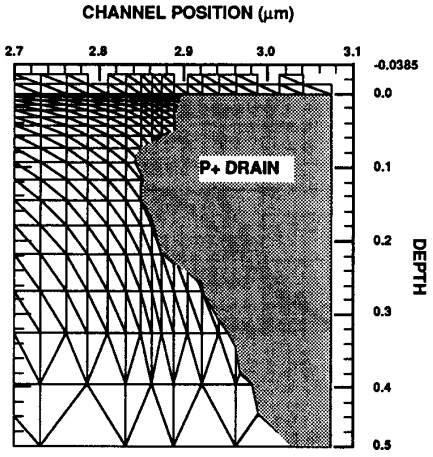

Figure 6: PISCES simulation mesh for the simulations of Figures 3b, 8, and 9.

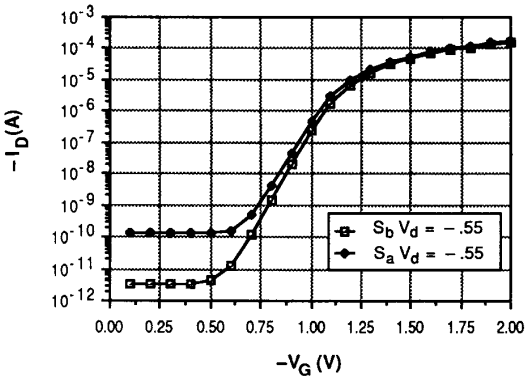

Figure 7: Measured I_D-V_G characteristic for the device of Figures 2-6 in the subthreshold regime. S_a and S_b are before and after DAHC stress, respectively.

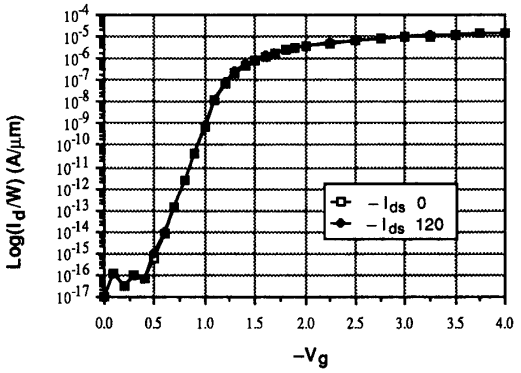

Figure 8: Simulated subthreshold characteristic using the mesh of Figure 6. Compare to Figure 7 by multiplying current values by the channel width W = 25μm.

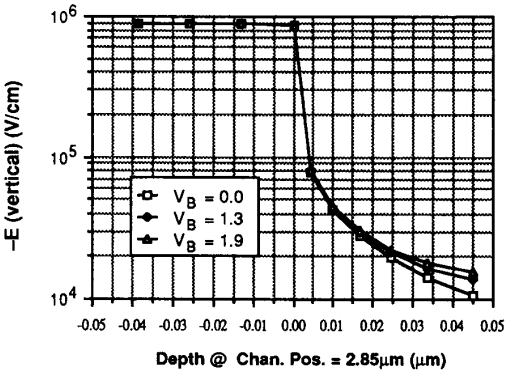

Figure 9: Simulated vertical electric field near the drain for the inversion portion (trap-filling) of the charge-pumping cycle ($V_G = -4.5V$). Changes in the vertical electric field are not large enough to explain the enhancment of I_{CP} reported in [5].