SUBSTRATE CURRENT IN N-CHANNEL AND P-CHANNEL MOSFETS BETWEEN 77K AND 300K: CHARACTERIZATION AND SIMULATION

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ABSTRACT

Silicon is the material of choice for fabrication of high circuit density, low defect density and high speed integrated devices. CMOS technology provides the additional advantage of low power dissipation. Performance enhancement can be obtained by operating CMOS circuits at liquid nitrogen temperatures [1]. However, low temperature operation exacerbates the generation of substrate current by impact ionization, leading to potential device degradation [2]. This work characterizes the temperature behavior of the substrate current, and presents a model describing this behavior based on Shockley's lucky electron (LE) model [3]. For N-channel (P-channel) devices, the model is extended using a Maxwell-Boltzmann (MB) distribution of hot electron (hole) energies above (below) the conduction (valence) band minimum (maximum). We implement the model in the 2-D device simulator CADDET [4]. The agreement between data and simulations enhances physical understanding of substrate current in MOSFETs, and warrants confident design of a CMOS technology for cryogenic operation.

INTRODUCTION

Accurate 2-D models of DC substrate current (I_B) are critical to CMOS device design for several reasons. Such a physical model would provide a foundation for development of an analytical model which could be utilized efficiently in a circuit simulator such as SPICE. More important, device reliability requires minimization of I_B [2]. In particular, I_B is far easier to monitor than gate current (I_G), or the amount and location of trapped oxide charge - yet it provides a measure of device degradation caused by I_G. Once I_B is well-predicted, one can move forward to the more complicated tasks of measuring and modelling I_G and insulator trapping and trap generation - toward a full, 2-D, DC device simulator.

In initiating this task, then, we have characterized I_B for a CMOS technology. Modelling efforts began with Shockley's LE model, along the lines of other workers (see **MODEL** section, below). However, one of our goals was to characterize the technology, to determine if reliability problems related to I_B would occur at liquid nitrogen temperature - that is, to determine if substrate current considerations would drive power supply voltages below a reasonable level for cryogenic operation. During these temperature measurements, it became clear the existing physical models were inadequate. We then used temperature as a tool to differentiate between appropriate, physical models. Finally, we used the model to address the issue of power supply voltage for a sub-micron, liquid nitrogen temperature CMOS technology, based on these I_B considerations.

EXPERIMENTAL DETAILS

CMOS transistors were fabricated in the Stanford IC Lab using a conventional N-well process [5], with t_{ox}= 385Å and .85 < L_e < 25μ. N+ poly and boron channel implants were used for both device types; the effect of the compensating implant in the P-channel is important [6], and is discussed further, below. The chosen implants yielded V_{TN} = .35V, and V_{TP} = -1.2V, for T = 293K. Low V_D transconductance and V_T were monitored before and after I-V measurements at each temperature, to ensure that the measurements did not degrade the device. Substrate current was measured for 0 < V_G < 5V , 1.5 < V_D < 5V and 77 < T < 300K. The N-channel devices use a standard As source-drain, with no LDD structure: as shown in previous work [7], N-channel LDD structures lead to serious problems for liquid nitrogen temperature (T_{LN}) operation, as trapped charge above the LDD region - combined with freezeout effects - turns off the device channel.

CHARACTERIZATION

The impact ionization process leading to the measurement of substrate current is shown in **Figure 1**, for an N-channel device. Channel electrons enter the high-field region of the device, acquiring enough energy to break a Si-Si bond (nominally E_g, the silicon band gap). A number of these carriers will, in fact, break a bond, generating free hole-electron pairs. The holes are swept into the body of the device, where they are measured as substrate current. A mirrored situation holds for P-channel devices.

Figure 2 shows I_B data for an N-channel FET with L_e = .85μ at 77K. Region **I** (V_G < V_T) indicates the expected exponential behavior of I_B : I_D is an exponential function of V_G in this region, and I_B is linearly related to I_D (see discussions of the model, below). Region **II** (V_D > V_G - V_T) is the peak substrate current regime, where the field in the pinch-off region (and, thus, the number of channel carriers with energy exceeding E_g) has reached a maximum, for a particular value of V_D. Region **III** (V_D < V_G - V_T) shows the expected decrease in I_B, as the device goes out of saturation and the field in the pinch-off region diminishes. An effective model must explain all three regions, over V_D as well as temperature.

In addition, any model must explain the effect first noted by Eitan, *et. al.* [8], and demonstrated for our N-channel devices. In **Figure 3**, we see that the peak I_B (normalized to I_D, to remove the temperature dependence of the channel current itself) for a device with L_e =1.15μ, DECREASES with decreasing temperature if V_D is low enough. This is precisely the effect one would want in a CMOS technology designed for cryogenic operation, to avoid hot carrier degradation effects. (Operation of a cryogenic CMOS technology above this critical supply voltage might also be possible, provided substrate currents and reliability problems associated with gate currents could be accurately predicted.) We call that V_D for which I_{BMAX} is roughly independent of temperature, V_{xover}.

We have extended Eitan's work, and plotted V_{xover} vs. L_e for our N-channel devices in **Figure 4**, from which one may infer a power supply voltage of less than 2V is required for a cryogenic CMOS technology designed so that hot carrier effects are no worse at low T than at room T. We note that we were unable to observe V_{xover} directly in our P-channel devices, due to a minimum measurable I_B in our system of roughly 100fA; however, extrapolation of our P-channel I_{BMAX} vs. T vs. V_D data is consistent with this 2V design requirement.

MODEL

Previously, a LE model was used successfully to predict I_B [9], as well as other NMOS effects [10]. One drawback of this model was its inability to predict the observation of V_{xover} (see **Figure**

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3). This work uses a MB distribution function to augment the previous model; **Figure 5** gives the rate equation, and explains the variables used. The electron temperature T_e [11] specifies the MB distribution. To describe both the I_B vs. V_G and I_{BMAX} vs. T curves, the model requires only a single fit parameter (which is the mean free path parameter, λ_0) for each device - over the entire range of V_G , V_D , L_e , and T . The values used for λ_0 in our process are 105Å for the N-channel, and 51.5Å for the P-channel devices.

Figure 6 demonstrates how the MB distribution can explain the observed V_{zover} . For the example shown, we assume a channel carrier has acquired 1V, and so requires an additional .1V to impact ionize a Si-Si bond. The first set of curves shows that the fractional number A_{MB} of carriers which have energy greater than .1V due to the high field for high V_D , is greater at 77K than at 300K. For high V_D , A_{MB} is nearly equal to unity, so that the impact ionization rate is controlled by the LE term alone. Since λ increases monotonically as T is decreased from 300K to 77K, the LE probablity, and thus the substrate current, increases with decreasing temperature.

The second set of curves demonstrate the situation for small V_D . Here, the value of A_{MB} departs significantly from unity, so that A_{MB} is less at 77K than at 300K. Thus, the impact ionization rate is controlled by both the LE as well as the MB probability terms in the rate equation, two mechanisms which compete. If the energy distribution term changes more rapidly than the LE term, we have the prediction of V_{zover} , just as is measured experimentally.

DISCUSSION

Figures 7-10 show comparisons between CADDET simulations using the model and our devices for a few of the temperatures and channel lengths measured. Space limits presentation of the full range of T and L_e ; but these good results - at the longest and shortest L_e , at the highest (300K) and lowest (77K) temperatures, for both device types - give an excellent description of the model's performance. In particular, V_{zover} is well-predicted (see **Figure 4**).

Nevertheless, some self-criticism of the model is in order. First, regarding underprediction of I_B at high V_G (see **Figure 8**, for instance), a MB distribution of energies may not be the correct one to use. However, abandoning the MB distribution would make the simulation task much more difficult, as Monte Carlo techniques become necessary to establish the energy distribution [12].

Second, low predictions for I_{BMAX} at the highest V_D could be the result of multiple impact ionization events from a single channel carrier; or, from subsequent impact ionizations caused by impact ionized (not channel) carriers [9].

We experienced some underprediction of P-channel I_B in the linear region (Region **I** in **Figure 2**). The problem arises even at low V_D for the long-channel device (**Figure 9**), and occurs because of a a problem with CADDET - underprediction of subthreshold I_D . For such low fields (low V_D , long L_e), Boltzmann statistics are insufficient to describe the Fermi levels in this (compensated) P-channel, even at 300K. That is, compensation and full Fermi-Dirac statistics will predict a hole quasi- Fermi level significantly closer to the valence band than Boltzmann statistics [6].

Finally, we have asserted that DC device degradation under stress will be proportional to I_B at low T as well as 300K (recall [2]). However, this has not been demonstrated experimentally; work is underway to fill this void in our knowledge.

CONCLUSION

We have characterized the substrate current in a CMOS technology over a wide range of channel lengths and bias voltages. The characterization has demonstrated the limits on power supply voltages - inferred from the relationship between I_B and device degradation - over the full temperature range, 77K to 300K.

A physical model to explain the experimental observations has been developed, based on the notion that carriers - due to high electric fields - can have energies significantly above their band minima. The model has been implemented in the 2-D device simulator CADDET. The model requires a minimum number of fit parameters (one per device type) to describe the observed I_B ; furthermore, because the model is based on a local knowledge of channel fields, voltages, and current densities, it is expected to be equally applicable to other technologies. The close agreement between model and experiment indicates that design and realization of a reliable, scaled, low temperature CMOS technology should not be hindered by an inordinately low power supply voltage.

ACKNOWLEDGEMENTS

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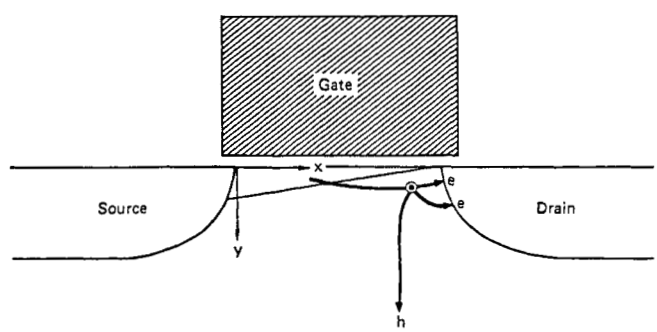


Figure 1. Schematic of impact ionization current, leading to measurement of substrate current, in an N-channel MOSFET.

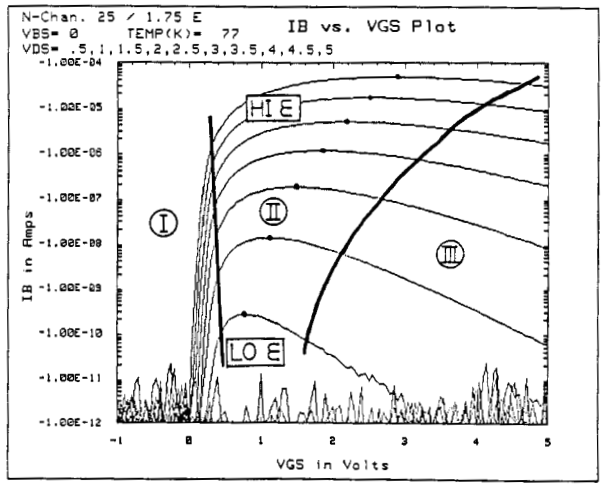


Figure 2. Substrate current vs. gate voltage for an N-channel MOSFET, at various drain voltages. $L_e = .85\mu$; $T = 77$K. HI and LO refer to V_D regions with different temperature coefficients for I_{BMAX} vs. T (see text for discussion).

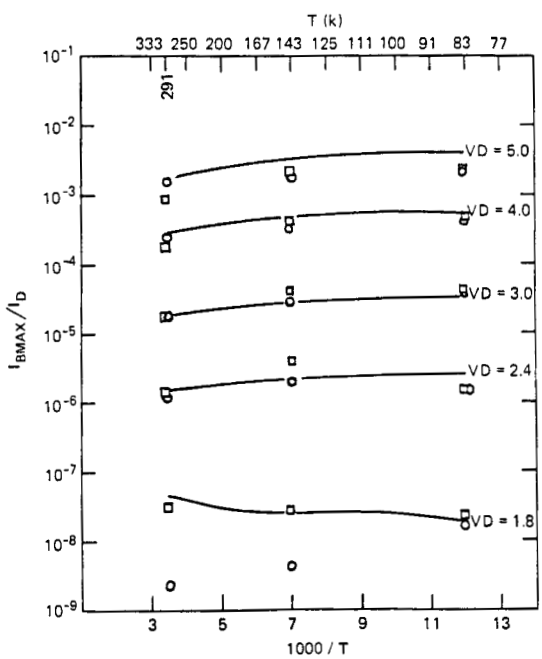


Figure 3. Peak substrate current vs. temperature for an N-channel MOSFET. $L_e = 1.15\mu$. o = LE model alone; □ = MB plus LE model.

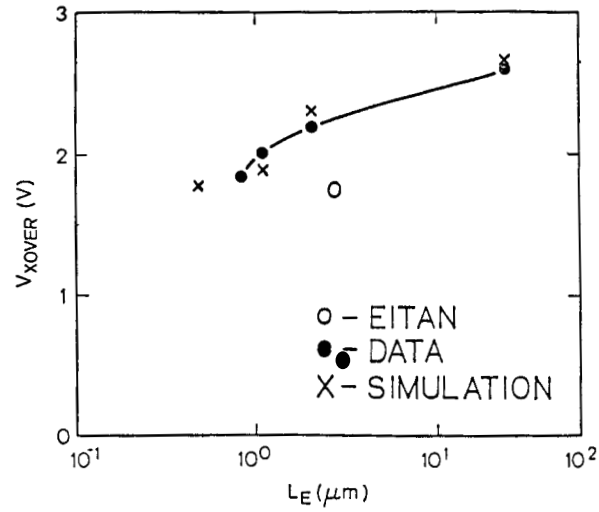
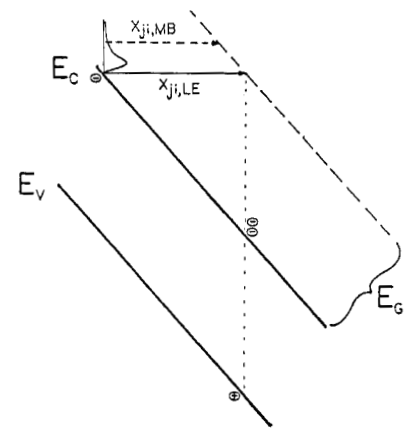


Figure 4. Crossover voltage vs. channel length for N-channel devices.



$$R_{ii,MB} \sim J_D \cdot \exp(-\frac{x_{ji}}{\lambda}) A_{MB}(E_g - V_{ji})$$

$$A_{MB}(E_g - V_{ji}) = \left\{ (\frac{E_g - V_{ji}}{kT_e} + 1) \exp[-\frac{(E_g - V_{ji})}{kT_e}] \right\}$$

$$T_e = (T/2)\{1 + [1 + (\frac{\mu \mathcal{E}_i}{v_s})^2]^{1/2}\} \qquad \lambda = \lambda_0 tanh(\frac{E_p}{2kT})$$

Figure 5. Schematic of the impact ionization model. V_{ji} is the energy acquired in traversing a path x_{ji} . The rate equation is summed over all starting points i and all final points j along a current path. Some carriers travel a shorter distance (x_{ji}) with the MB model in acquiring the energy E_g to break a Si-Si bond, than with the LE model alone - which can increase or decrease R_{ii} , depending upon whether V_D is, respectively, HI or LO. E_p is the optical phonon energy, discussed in [3].

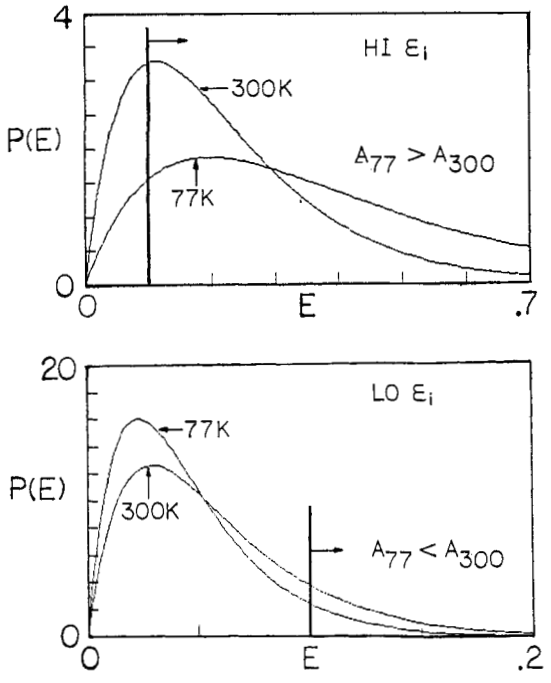


Figure 6. How V_{xover} is predicted by an energy distribution. The probability curves are normalized for unity area. See text for discussion.

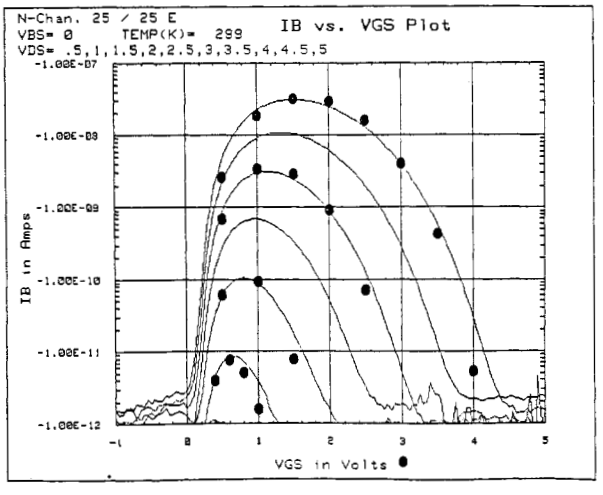


Figure 7. Substrate current vs. gate voltage for 25/25 N device at T =299K. Simulation results shown by •••.

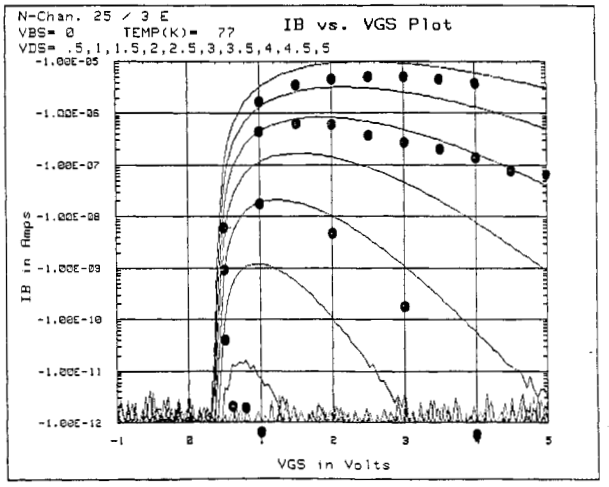


Figure 8. Substrate current vs. gate voltage for 25/3 N device at T =77K. L_e =2.15μ. Simulation results shown by •••.

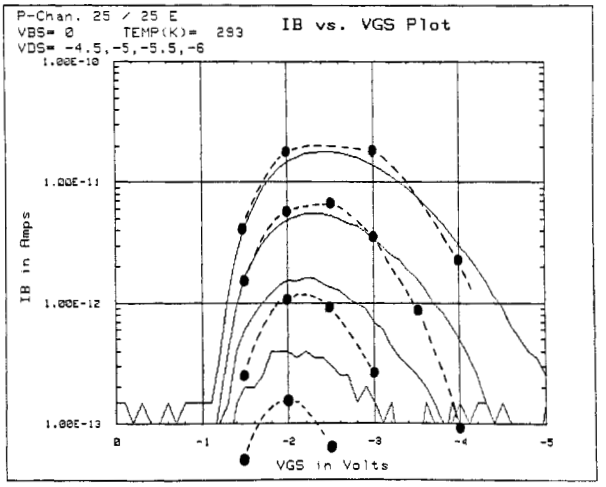


Figure 9. Substrate current vs. gate voltage for 25/25 P device at T =294K. Simulation results shown by •••.

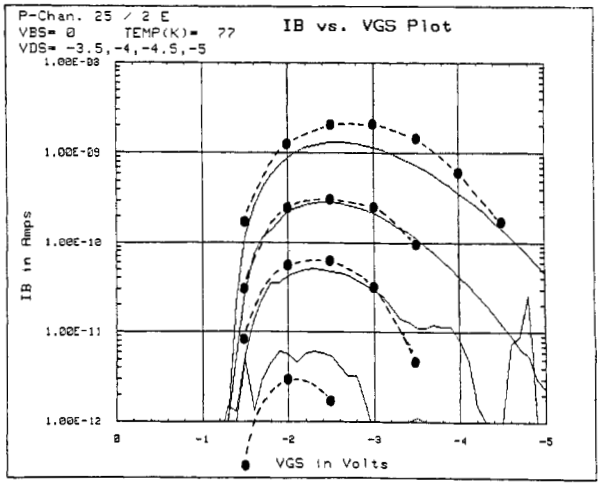


Figure 10. Substrate current vs. gate voltage for 25/2 P device at T =77K. L_e =1.17μ. Simulation results shown by •••.