incorporates the effects of ESA and pump-induced depletion of the metastable level.

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CALCULATION OF LATERAL DISTRIBUTION OF INTERFACE TRAPS ALONG MIS CHANNEL

Indexing terms: Semiconductor devices and materials, Metal-oxide semiconductor structures and devices

The lateral distribution of interface traps, averaged over the semiconductor band gap, is calculated in an MIS structure. The calculation is based on the well known charge-pumping technique. The calculation has been applied to *p*-channel MOSFETs.

Introduction: Understanding the location of interface trap generation in MOSFETs under stress has become critical for building reliability into device operation at the microscopic design level. Interface traps cause direct changes in transconductance, subthreshold slope, and noise figure.[1–4] They are also indirect evidence of hot carriers in MOSFETs, and can aid in creating physical, microscopic models of hot carrier transport.

In MOSFETs, interface traps have been characterised in three ways: as an average value over both the surface energy bandgap and channel length N_{it} (cm^{-2}),[5,6] as an average over the band gap, but not channel length, $N_{it}(x)$ (cm^{-2}),[6] and as an average over channel length, but not surface potential energy in the band gap, $D_{it}(\Psi)$ ($eV^{-1}\,cm^{-2}$).[7–9] (No work to date has looked at the full $D_{it}(x, \Psi)$.)

Lately, the method of choice for characterisation of interface traps has been the charge-pumping technique.[6,10,11] In particular, we develop here an alternate method to Reference 7 for finding $N_{it}(x)$ (cm^{-2}). As before, the method is based on profiling the interface traps against position near the drain by varying the junction reverse bias. Peak charge-pumping current is measured against reverse junction bias. Increasing reverse bias causes the source-drain space-charge regions to grow. Their extension effectively reduces the channel length. For charge-pumping applications, this means a smaller channel area will contribute to the charge-pumping current. Any interface traps located in the depleted region will be effectively masked and unable to contribute to I_{cp}. The combination of changes in I_{cp} and channel length are used to extract $N_{it}(x)$ against position along the channel. This alternate method appears simpler than the previous one, as shown in the derivation below; at the same time, it avoids the crucial assumption of constant $N_{it}(x)$ in prestressed devices made in Reference 7.

Several assumptions are made. First, any damage, i.e. interface trap generation, is assumed to occur only on the drain side of the channel. Therefore, the interface trap distribution on the source side is assumed to be the same before and after stress. Secondly, the spatial distributions of interface traps are assumed to be the same (not necessarily constant) on both source and drain sides, prior to any stress.

To begin the derivation, energy-averaged interface traps may be expressed as

$$N_{it}(x) = \int_{E_v}^{E_c} D_{it}(x, \Psi)\, d\Psi \tag{1}$$

That is, the surface potential Ψ, controlled by the gate bias of the charge-pumping measurement, is assumed to span the entire semiconductor bandgap. The energy-averaged interface traps then come from integrating $D_{it}(x, \Psi)$ over this bandgap.

The charge-pumping current I_{cp} is calculated according to

$$I_{cp} = q\,.\,f\,.\,W \int_{-L(V_r)/2}^{L(V_r)/2} dx \int_{E_v}^{E_c} D_{it}(x, \Psi)\, d\Psi \tag{2}$$

Charge q, frequency f, and MOSFET channel width W control part of I_{cp}. The two integrals take $D_{it}(x, \Psi)$ into account, adding up contributions across the bandgap and along the channel. Note that the reverse-bias-dependent source depletion edge is defined to be at $x = -L(V_r)/2$, with the drain edge at $+L(V_r)/2$. Thus, the centre of the channel is defined to be $x = 0$, and is independent of V_r.

$N_{it}(x)$ for an unstressed device can be found using these equations. Define the unstressed charge-pumping current I_{cp0} as

$$I_{cp0} = 2\,.\,q\,.\,f\,.\,W \int_{0}^{L(V_r)/2} dx N_{it0}(x) \tag{3}$$

Here, the factor of 2 and the change of the lower limit of the integral stem from the assumption of $N_{it}(x)$ being symmetric at source and drain for the unstressed device.

Taking the derivative with respect to L of I_{cp0} will allow calculation of $N_{it0}(x)$.

$$\frac{dI_{cp0}}{dL} = 2\,.\,q\,.\,f\,.\,W\,.\,\frac{d}{2\,.\,d\left(\frac{L}{2}\right)} \times \int_{0}^{L(V_r)/2} dx N_{it0}(x) \tag{4}$$

$$= q\,.\,f\,.\,W\,.\,N_{it0}\left(\frac{L}{2}\right) \tag{5}$$

Inverting this last equation, and applying the chain rule $(d/dL = \{d/dV\}\{dV/dL\})$

$$N_{it0}\left(\frac{L}{2}\right) = \frac{1}{q \cdot f \cdot W} \frac{dI_{cp0}}{dV_r} \frac{dV_r}{dL} \tag{6}$$

Measurements of dI_{cp0}/dV_r, and measurements or simulation of dV_r/dL, thus allow extraction of $N_{it0}(x)$, where $x = L/2$ and is dependent on the applied reverse bias.

For a device after stress, $N_{it}(x)$ near the drain (injection region) no longer looks like its counterpart $N_{it0}(x)$ near the source. Proceeding as before

$$I_{cp} = q \cdot f \cdot W \int_{-L(V_r)/2}^{L(V_r)/2} dx N_{it}(x) \tag{7}$$

$$= q \cdot f \cdot W \times \left[\int_{-L(V_r)/2}^{0} dx N_{it}(x) + \int_{0}^{L(V_r)/2} dx N_{it}(x) \right] \tag{8}$$

Because the first integral in eqn. 8 is over the unstressed part of the channel, we may convert it to

$$\int_{-L(V_r)/2}^{0} dx N_{it}(x) = \int_{-L(V_r)/2}^{0} dx N_{it0}(x) = \int_{0}^{L(V_r)/2} dx N_{it0}(x) \tag{9}$$

Making this substitution, and taking the derivative again with respect to channel length L, we obtain

$$\frac{dI_{cp}}{dL} = q \cdot f \cdot W \times \left[\frac{d}{2 \cdot d\left(\frac{L}{2}\right)} \int_{0}^{L(V_r)/2} dx N_{it0}(x) + \frac{d}{2 \cdot d\left(\frac{L}{2}\right)} \int_{0}^{L(V_r)/2} dx N_{it}(x) \right] \tag{10}$$

$$= \frac{q \cdot f \cdot W}{2} \left[N_{it0}\left(\frac{L}{2}\right) + N_{it}\left(\frac{L}{2}\right) \right] \tag{11}$$

where the last step, as before, results from the derivative with respect to the limit of a definite integral. Rearranging, and using the chain rule one last time, gives the final result

$$N_{it}\left(\frac{L}{2}\right) = \frac{2}{q \cdot f \cdot W} \frac{dI_{cp}}{dV_r} \frac{dV_r}{dL} - N_{it0}\left(\frac{L}{2}\right) \tag{12}$$

Application: The following experimental measurements and analysis steps are needed to evaluate $N_{it}(x)$:

(1) obtain I_{cp} against V_r data before and after stress

(2) calculate dI_{cp}/dV_r

(3) determine L against V_r with a one- or two-dimensional approximation, or by measurement

(4) calculate dL/dV_r (using a curve fit from L against V_r)

(5) calculate N_{it} against V_r from the I_{cp} data obtained

(6) calculate $N_{it}(x)$ from eqn. 12.

We have applied the technique to the determination of lateral interface traps in p-channel MOSFETs.[12] PISCES[13] was used to establish carrier density against lateral position along the interface, as a function of reverse junction bias. This was necessary to determine the channel length, defined by the depletion edge in the channel, as a function of reverse bias. Care was taken to identify the location of the depletion edge, as discussed elsewhere.[14]

Fig. 1 shows the experimental setup. Fig. 2 shows the results of applying the new method to measurements on a pMOS transistor.

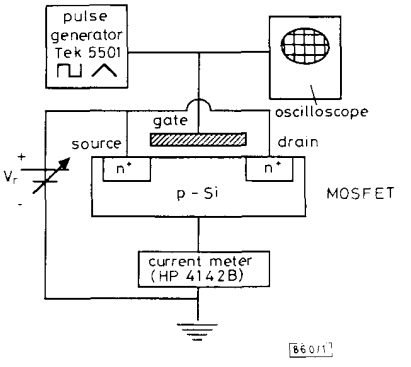

Fig. 1 *Schematic diagram of charge-pumping measurement setup*
Polarities for pMOS devices measured in this work are reversed from the Figure

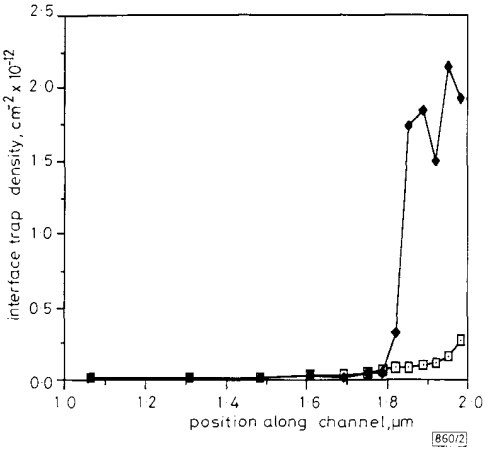

Fig. 2 *Interface trap density $N_{it}(x)$ against channel position, before and after stress, for pMOSFET with $W = 25\,\mu m$, $L_{eff} = 1{\cdot}7\,\mu m$ (300 K)*
Drain metallurgical junction is located at 1·78 μm on scale above
□ Prestress trap density
◆ post-stress trap density
Stress condition was 120 min, $V_{DS} = -10$ V, $V_{GS} = -2{\cdot}5$ V

Discussion: The new technique employed here allows determination of interface trap density, averaged over the bandgap, as a function of position along the FET channel, regardless of whether the device has been stressed or not. That is, no assumption is made of uniform $N_{it}(x)$ in the unstressed device, as in Reference 7. We note allusion to a technique was made in Reference 9. However, no calculations were presented in that work, which led us to attempt them independently, with the results presented above.

Our calculated $N_{it}(x)$ in the pMOS FET (Fig. 2) reveals similarities to the nMOS device results presented in Reference

9, both before and after stress, as we have discussed elsewhere.[12] In particular, we note a nonuniform interface trap density near the junctions of the unstressed device. We believe this is due to enhanced interface trap densities above heavily-doped junction regions. An alternative explanation exists for the increase;[9] that is, electric field-enhanced emission of trapped charges near junctions, rather than increased numbers of interface traps. Simulations of vertical field near the drain junction[12] appear to refute this explanation, leaving heavy doping effects as the likely candidate.

Conclusions: We have derived a new method for calculating lateral interface trap densities in MIS devices, based on measurements of charge-pumping current against junction reverse bias. The new method improves on previous ones by eliminating the critical assumption of uniform trap density prior to device stress. The method thus can be used to find lateral interface trap densities in unstressed devices. We have applied the new method to *p*MOS FETs, and obtained results similar to those reported in *n*MOS transistors.

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REPRESSION AND SPEED IMPROVEMENT OF PHOTOGENERATED CARRIER INDUCED REFRACTIVE NONLINEARITY IN InGaAs/InGaAsP QUANTUM WELL WAVEGUIDE

Indexing terms: Waveguides, Nonlinear optics, Semiconductor devices and materials

For the first time, the all-optical refractive nonlinearity due to photogenerated carriers in an InGaAs/InGaAsP quantum well waveguide under various bias conditions is measured. With no bias, the nonlinearity has a slow recovery time, of the order of the recombination time of the carriers. For a coupled power of 4·3 W and a 600 μm long device, we measure a phase modulation of $7{\cdot}5 \pm 2$ radians. Under forward bias the nonlinearity is effectively quenched. Under reverse bias the nonlinearity remains, although slightly reduced. In the latter case the recovery time is dramatically reduced to approximately 50 ps.

Introduction: All-optical nonlinearities in semiconductor optical waveguides are of interest because they have the potential for applications in ultrafast optical switching. However, it has been shown that absorption of photons, creating electron-hole pairs, may have a deleterious effect on the all-optical switching characteristics of a nonlinear waveguide device.[1,2] The photogenerated electron-hole pairs have recombination lifetimes of the order of 1 ns in InGaAsP materials and hence any refractive nonlinearity caused by the presence of carriers has a relatively long recovery time. This limits the usefulness of any device that uses such a nonlinearity unless a method is found for removing them quickly.

Electron-hole pairs may be generated by a variety of physical mechanisms as light passes through a waveguide. At a wavelength close to the bandedge of the material, the main mechanism is linear absorption. At high light intensities other mechanisms, such as two photon absorption (TPA), may become significant.

This Letter reports the measurement of the selfphase modulation (SPM) that arises from the refractive nonlinearity enhanced by photogenerated carriers in an InGaAs/InGaAsP quantum well waveguide. Both the magnitude and speed of response of the SPM are ascertained for a range of electrical bias conditions. In particular, we show that there is a significant decrease in recovery time under reverse bias conditions when carriers are swept out of the intrinsic region.

Device construction: The structure of the device was a *pin* ridge waveguide. Fabrication was by MOCVD on a [001] orientated n^+ InP substrate on which was grown an InP *n* layer and a 0·27 μm thick nominally intrinsic InGaAsP waveguide layer. Five nominally intrinsic InGaAs quantum wells, of thickness 6 nm, were grown within this layer. The wells were separated by 10 nm wide barrier layers. A *p* layer of InP and a p^+ capping layer of InGaAs were grown on top of the waveguide region. A 3·5 μm wide ridge was etched onto the device to provide transverse guiding. Metal contacts were deposited on the *p* and *n* sides, an oxide layer allowing current injection in the ridge alone. The device was 600 μm long and its cleaved facets were antireflection coated to eliminate Fabry–Perot effects.

Experiment: Fig. 1 shows the experimental arrangement used for measuring SPM in the waveguide. A KCl : Tl colour centre laser, which could either be operated CW or mode-locked, was pumped by a mode-locked Nd : YAG laser. The wavelength of the colour centre laser was tuned to 1·53 μm, reasonably close to the photoluminescence peak at 1·48 μm. The duration of the mode-locked pulses from the colour centre laser was measured using an SHG autocorrelator and was found to be 30 ps FWHM. The power incident on the waveguide was varied by the use of a halfwave plate and a polariser combination which was also used to select the polarisation of the light to be TE (parallel to the waveguide layer). An 18 × microscope objective lens was used to couple light into the guide. Singlemode injection into the waveguide